CBCS Scheme

USN | | | | | | | | | | 15CS32

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: *Answer FIVE full questions, choosing one full question from each module.*

Module-1

1 a. Explain the working of N – channel DE – MOSFET, with the help of neat diagram. **(08 Marks)**

b. With circuit diagram, explain any two application of FET. **(06 Marks)**

c. How CMOS can be used as inverting switch? **(02 Marks)**

OR

2 a. Design a voltage divider bias network using a DEMOSFET with supply voltage $V_{DD} = 16V$, $I_{DSS} = 10mA$ and $V_P = 5V$ to have a quiescent drain current of 5mA and gate voltage of 4V. (Assume the drain resistor R_D to be four times the source resistor R_S and $R_2 = 1k\Omega$). **(08 Marks)**

b. Explain the performance parameters of Op-amp. **(08 Marks)**

Module-2

3 a. Minimize the following Boolean function using K – map method
$f(a, b, c, d) = \Sigma m (5, 6, 7, 12, 13) + \Sigma d (4, 9, 14, 15)$. **(06 Marks)**

b. Apply Quine Mc – Clusky method to find the essential prime implicants for the Boolean expression $f(a, b, c, d) = \Sigma m (1, 3, 6, 7, 9, 10, 12, 13, 14, 15)$. **(10 Marks)**

OR

4 a. A digital system is to be designed in which the month of the year is given as input is four bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess number in the input beyond '1011' as don't care conditions for the system of four variables. (ABCD) find the following :
i) Write truth table and Boolean expression in SOP Σm and POS ΠM form.
ii) Using K – map simplify the Boolean expression of canonical mini term form.
iii) Using Basic gates implement logical circuit. **(10 Marks)**

b. What is Hazard? List the type of hazards and explain static 0 and static – 1 hazard. **(06 Marks)**

Module-3

5 a. Implement the following function using 8:1 multiplexer $f(a, b, c, d) = \Sigma m (0, 1, 5, 6, 8, 10, 12, 15)$. **(06 Marks)**

b. Realize the following function using 3:8 decoder
i) $f(a, b, c) = \Sigma m (1, 2, 3, 4)$ ii) $f(a, b, c) = \Sigma m(3, 5, 7)$. **(04 Marks)**

c. What is Magnitude Comparator? Explain 1 bit magnitude comparator. **(06 Marks)**

OR

6 a. Design 7 – segment decoder using PLA. **(08 Marks)**

b. Differentiate between Combinational and Sequential circuit. **(04 Marks)**

c. Write VHDL code for given circuit. **(04 Marks)**

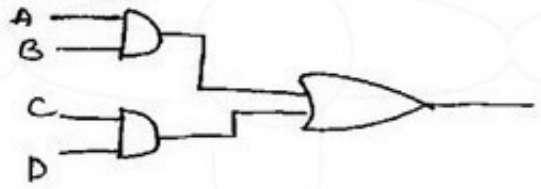

Fig.Q6(c)

Module-4

7 a. What is Race around condition? With block diagram and truth table, explain the working of JK master – slave flip – flop. **(10 Marks)**

b. Give State transition diagram and characteristics equation for JK and SR Flip Flop. **(06 Marks)**

OR

8 a. With neat diagram, explain Ring counter. **(04 Marks)**

b. What is Shift Register? With neat diagram, explain 4 bit parallel in serial out shift resisters. **(08 Marks)**

c. Compare Synchronous and Asynchronous counter. **(04 Marks)**

Module-5

9 a. Define Counter. Design A synchronous counter for the sequence $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$ using JK Flip – Flop. **(12 Marks)**

b. Explain Digital clock, with neat diagram. **(04 Marks)**

OR

10 a. Explain the Binary ladder with Digital input of 1000. **(06 Marks)**

b. Explain 2 bit simultaneous A/D converter. **(10 Marks)**

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15CS32

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Analog and Digital Electronics (ADE)

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Explain the operation and characteristics of N-channel JFET. **(08 Marks)**

b. With block diagram, explain the operation of a Astable multivibrator using IC 555. **(08 Marks)**

OR

2 a. With circuit diagram, explain the operation of a Relaxation oscillator. **(06 Marks)**

b. Fig. Q2(b), shows a Biasing configuration using DEMOSFET given that the saturation drain current is 8mA and the pinch off voltage is -2V.

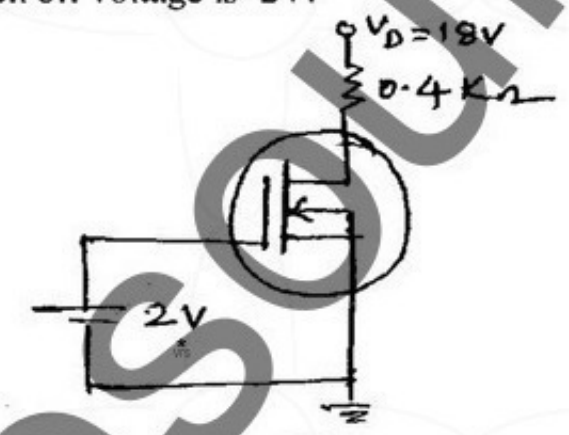

Fig. Q2(b)

Determine the value of gate source voltage drain current of drain source voltage. **(06 Marks)**

c. Write the advantages of MOSFET over JFET. **(04 Marks)**

Module-2

3 a. Give the simplest logic circuit for following logic equation where d represents don't care condition for following locations:

$F(A, B, C, D) = \sum m(7) + d(10, 11, 12, 13, 14, 15)$. **(06 Marks)**

b. Simplify the following Boolean function by using Quine – McClusky method.

$F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$. **(10 Marks)**

OR

4 a. What are Hazards? Explain the types of Hazards and it covers. **(08 Marks)**

b. Discuss Briefly an HDL Implementation models. **(04 Marks)**

c. Explain the concept of Duality in Digital circuits. **(04 Marks)**

Module-3

5 a. What is multiplexer? Design a 32:1 multiplexer using 16:1 MUX and one 2:1 multiplexer. **(05 Marks)**

b. Show how using a 3 to 8 Decoder and multi input OR Gates following Boolean Expressions can be realized simultaneously. **(06 Marks)**
$F(A, B, C) = \sum m (0, 4, 6)$
$F(A, B, C) = \sum m (1, 2, 3, 7)$
$F(A, B, C) = \sum m (0, 5)$

c. Show how two 1 to 16 DEMUX can be connected to get 1 to 32 DEMUX. **(05 Marks)**

OR

6 a. Explain parity Generators and checkers using suitable examples. **(05 Marks)**

b. What is Magnitude Comparator? Explain 1 bit magnitude comparator. **(05 Marks)**

c. What is PLA? Design seven segment Display using PLA. **(06 Marks)**

Module-4

7 a. Explain 4 bit serial in parallel out register. **(04 Marks)**

b. Explain a 3 bit binary Ripple up counter. Give the block diagram, truth table and output waveforms. **(06 Marks)**

c. Explain the working of JK master slave Flip Flop along with implementation using NAND Gates. **(06 Marks)**

OR

8 a. Design synchronous MOD – 6 counter with truth table and state diagram. **(06 Marks)**

b. What is universal shift Register? Explain any one application of universal shift register with block diagram and truth table. **(06 Marks)**

c. Write the comparison between Synchronous and Asynchronous counter. **(04 Marks)**

Module-5

9 a. Explain 5 bit Resistive divider with diagram. **(06 Marks)**

b. Explain with neat diagram the working principle of Digital clock. **(05 Marks)**

c. Explain the terms Accuracy and Resolution for D/A converter. **(05 Marks)**

OR

10 a. Explain with Block diagram the operation of successive approximation converter. **(08 Marks)**

b. Explain counter type A/D converter with diagram. **(08 Marks)**

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15CS32

Third Semester B.E. Degree Examination, June/July 2017
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Explain with help of a circuit diagram and characteristic curves working of N-channel DE MOSFET. **(12 Marks)**

b. List and explain any one application of FET and its working with circuit Diagram. **(04 Marks)**

OR

2 a. Explain the performance parameters of operational amplifier. **(08 Marks)**

b. Mention and explain the working of any two applications of operational amplifier. **(08 Marks)**

Module-2

3 a. What is a logical gate? Realize $((A + B) \cdot C)D$ using only NAND Gates. **(04 Marks)**

b. Describe positive and Negative logic. List the equivalences between them. **(04 Marks)**

c. Find the minimal SOP (sum of product) for the following Boolean functions using K-map

i) $f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11)$

ii) $f(a, b, c, d) = \pi M(1, 2, 3, 4, 10) + d(0, 15)$ **(08 Marks)**

OR

4 a. Using Quine – MCClusky Method simplify the following Boolean equation.
$f(a, b, c, d) = \sum m(0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$. **(10 Marks)**

b. Define Hazard. Explain Different Types of Hazards. **(06 Marks)**

Module-3

5 a. What is multiplexer? Design a 32 to 1 multiplexer (MUX) using two 16 to 1 MUX and one 2 to 1 MUX. **(04 Marks)**

b. Show How using 3 to 8 Decoder and multi input OR gates, following Boolean Expressions can be realized simultaneously
$F_1(a, b, c) = \sum m(0, 4, 6)$, $F_2(a, b, c) = \sum m(0, 5)$, $F_3(a, b, c) = \sum m(1, 2, 3, 7)$ **(05 Marks)**

c. Design 7 segment Decoder using PLA. **(07 Marks)**

OR

6 a. Implement the Boolean function expressed by SOP $f(a, b, c, d) = \sum m(1, 2, 5, 6, 9, 12)$ using 8 : 1 MUX. **(04 Marks)**

b. What is magnitude comparator? Design and explain 2 bit magnitude comparator. **(08 Marks)**

c. Differentiate between combinational and sequential circuit. **(04 Marks)**

Module-4

7 a. With a neat logic diagrams and truth table. Explain the working of JK master slave Flip-Flop along with its implementation using NAND Gates. **(10 Marks)**

b. Derive the characteristic equation for SR, D and JK Flip-Flop. **(06 Marks)**

OR

8 a. Using Negative Edge triggered D-Flip Flop. Draw a Logic diagram of 4 bit serial in serial out (SISO) Register. Draw the waveform to shift Binary number 1010 into this register. **(06 Marks)**

b. Explain with neat diagram How shift Register can be applied for serial addition. **(07 Marks)**

c. Differentiate between synchronous and Asynchronous counter. **(03 Marks)**

Module-5

9 a. Design Asynchronous counter for the sequences $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$. Using S. R Flip-Flop. **(12 Marks)**

b. With neat diagram. Explain Digital Clock. **(04 Marks)**

OR

10 a. Explain 2 bit simultaneous A/D converter. **(10 Marks)**

b. What is Binary Ladder? Explain the Binary Ladder with Digital input of 1000. **(06 Marks)**

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